# 2N3055(NPN), MJ2955(PNP)

**Preferred Device**

# Complementary Silicon Power Transistors

Complementary silicon power transistors are designed for general−purpose switching and amplifier applications.

### Features

- DC Current Gain − $h_{FE}$ = 20−70 @ $I_C$ = 4 Adc
- Collector−Emitter Saturation Voltage − $V_{CE(sat)}$ = 1.1 Vdc (Max) @ $I_C$ = 4 Adc
- Excellent Safe Operating Area
- Pb−Free Packages are Available*

### MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Collector−Emitter Voltage | $V_{CEO}$ | 60 | Vdc |
| Collector−Emitter Voltage | $V_{CER}$ | 70 | Vdc |
| Collector−Base Voltage | $V_{CB}$ | 100 | Vdc |
| Emitter−Base Voltage | $V_{EB}$ | 7 | Vdc |
| Collector Current − Continuous | $I_C$ | 15 | Adc |
| Base Current | $I_B$ | 7 | Adc |
| Total Power Dissipation @ $T_C$ = 25°C<br>Derate Above 25°C | $P_D$ | 115<br>0.657 | W<br>W/°C |
| Operating and Storage Junction Temperature Range | $T_J$, $T_{stg}$ | −65 to +200 | °C |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

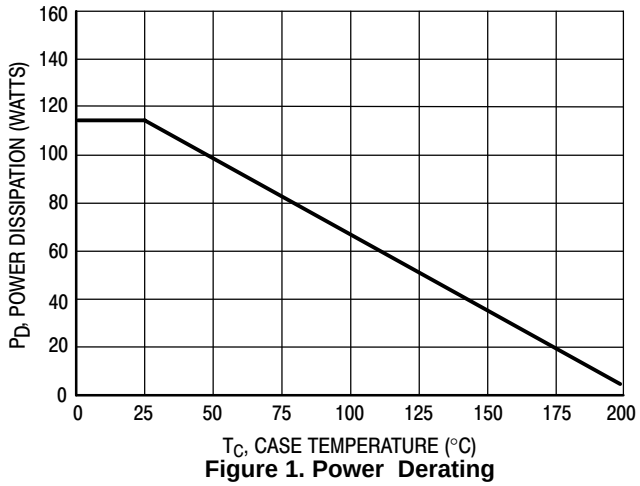


**Figure 1. Power Derating**

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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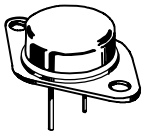
**http://onsemi.com**

## 15 AMPERE POWER TRANSISTORS COMPLEMENTARY SILICON 60 VOLTS, 115 WATTS



**TO−204AA (TO−3)**
**CASE 1−07**
**STYLE 1**

### MARKING DIAGRAM


xxxx55 = Device Code
xxxx = 2N30 or MJ20
G = Pb−Free Package
A = Location Code
YY = Year
WW = Work Week
MEX = Country of Orgin

### ORDERING INFORMATION

| Device | Package | Shipping |
|---|---|---|
| 2N3055 | TO−204AA | 100 Units / Tray |
| 2N3055G | TO−204AA (Pb−Free) | 100 Units / Tray |
| MJ2955 | TO−204AA | 100 Units / Tray |
| MJ2955G | TO−204AA (Pb−Free) | 100 Units / Tray |

**Preferred** devices are recommended choices for future use and best overall value.

**THERMAL CHARACTERISTICS**

| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| Thermal Resistance, Junction−to−Case | $R_{\theta JC}$ | 1.52 | °C/W |

**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| **OFF CHARACTERISTICS*** | | | | |
| Collector−Emitter Sustaining Voltage (Note 1) ($I_C$ = 200 mAdc, $I_B$ = 0) | $V_{CEO(sus)}$ | 60 | − | Vdc |
| Collector−Emitter Sustaining Voltage (Note 1) ($I_C$ = 200 mAdc, $R_{BE}$ = 100 Ω) | $V_{CER(sus)}$ | 70 | − | Vdc |
| Collector Cutoff Current ($V_{CE}$ = 30 Vdc, $I_B$ = 0) | $I_{CEO}$ | − | 0.7 | mAdc |
| Collector Cutoff Current<br>($V_{CE}$ = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc)<br>($V_{CE}$ = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc, $T_C$ = 150°C) | $I_{CEX}$ | <br>−<br>− | <br>1.0<br>5.0 | mAdc |
| Emitter Cutoff Current ($V_{BE}$ = 7.0 Vdc, $I_C$ = 0) | $I_{EBO}$ | − | 5.0 | mAdc |
| **ON CHARACTERISTICS*** (Note 1) | | | | |
| DC Current Gain<br>($I_C$ = 4.0 Adc, $V_{CE}$ = 4.0 Vdc)<br>($I_C$ = 10 Adc, $V_{CE}$ = 4.0 Vdc) | $h_{FE}$ | <br>20<br>5.0 | <br>70<br>− | − |
| Collector−Emitter Saturation Voltage<br>($I_C$ = 4.0 Adc, $I_B$ = 400 mAdc)<br>($I_C$ = 10 Adc, $I_B$ = 3.3 Adc) | $V_{CE(sat)}$ | <br>− | <br>1.1<br>3.0 | Vdc |
| Base−Emitter On Voltage ($I_C$ = 4.0 Adc, $V_{CE}$ = 4.0 Vdc) | $V_{BE(on)}$ | − | 1.5 | Vdc |
| **SECOND BREAKDOWN** | | | | |
| Second Breakdown Collector Current with Base Forward Biased<br>($V_{CE}$ = 40 Vdc, t = 1.0 s, Nonrepetitive) | $I_{s/b}$ | 2.87 | − | Adc |
| **DYNAMIC CHARACTERISTICS** | | | | |
| Current Gain − Bandwidth Product ($I_C$ = 0.5 Adc, $V_{CE}$ = 10 Vdc, f = 1.0 MHz) | $f_T$ | 2.5 | − | MHz |
| *Small−Signal Current Gain ($I_C$ = 1.0 Adc, $V_{CE}$ = 4.0 Vdc, f = 1.0 kHz) | $h_{fe}$ | 15 | 120 | − |
| *Small−Signal Current Gain Cutoff Frequency ($V_{CE}$ = 4.0 Vdc, $I_C$ = 1.0 Adc, f = 1.0 kHz) | $f_{hfe}$ | 10 | − | kHz |

*Indicates Within JEDEC Registration. (2N3055)

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

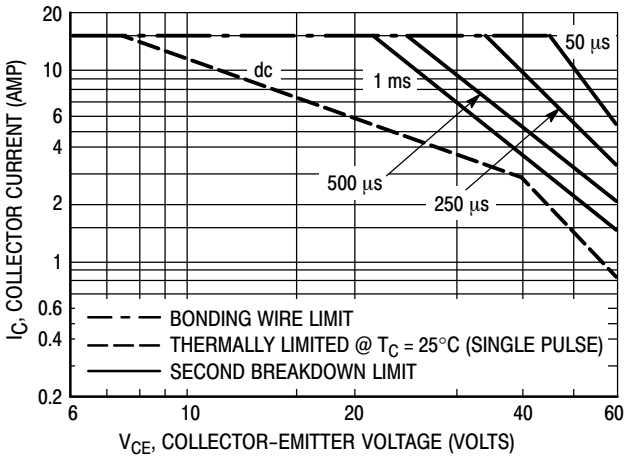



**Figure 2. Active Region Safe Operating Area**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_C$ = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated for temperature according to Figure 1.

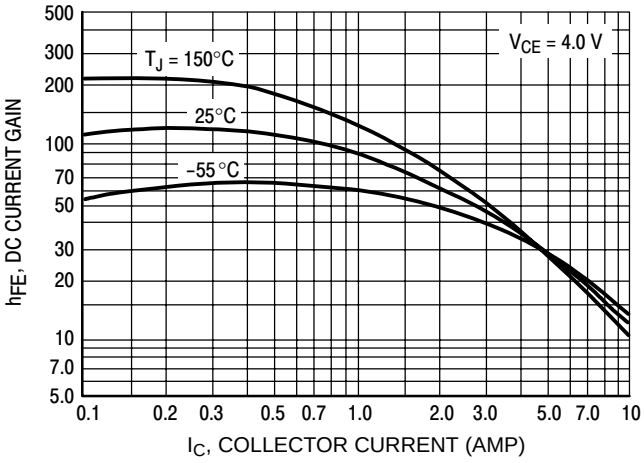



**Figure 3. DC Current Gain, 2N3055 (NPN)**

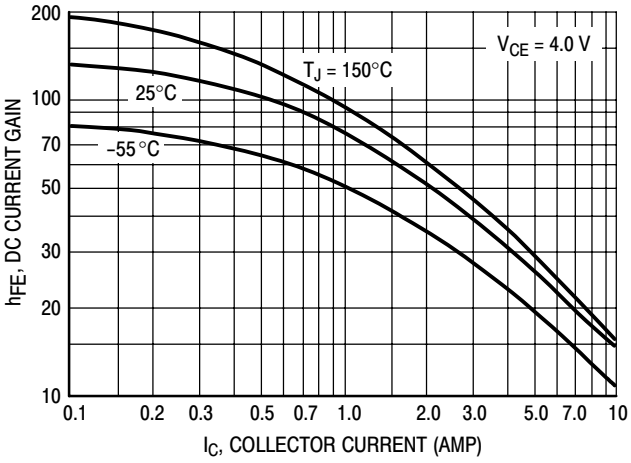



**Figure 4. DC Current Gain, MJ2955 (PNP)**

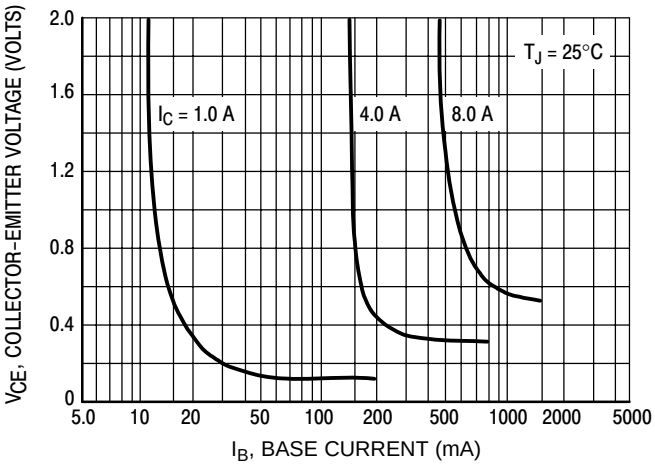



**Figure 5. Collector Saturation Region, 2N3055 (NPN)**

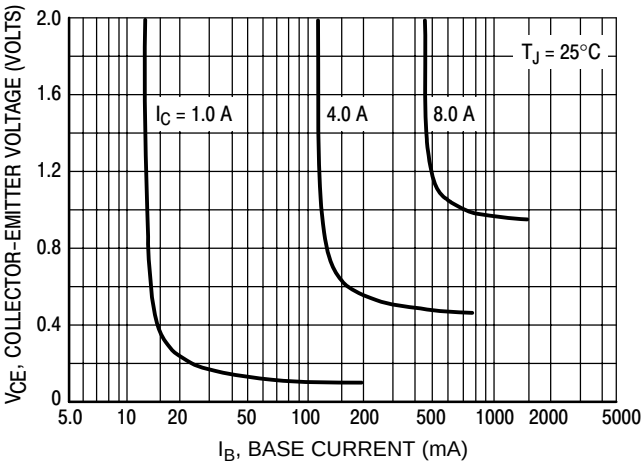



**Figure 6. Collector Saturation Region, MJ2955 (PNP)**

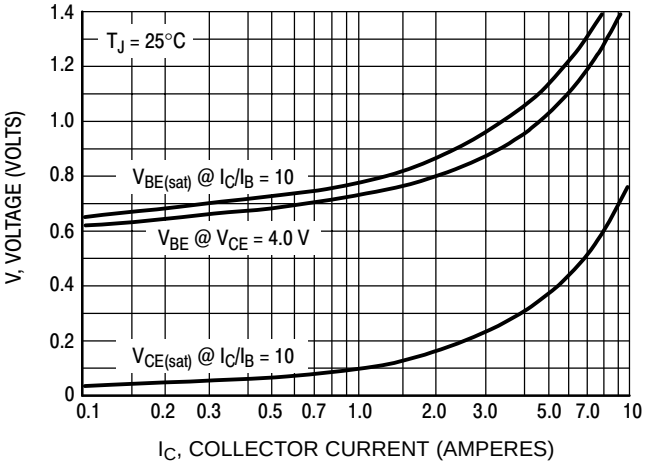



**Figure 7. “On” Voltages, 2N3055 (NPN)**

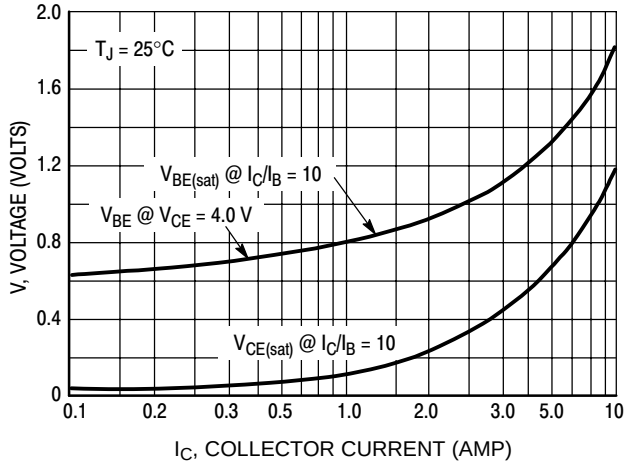
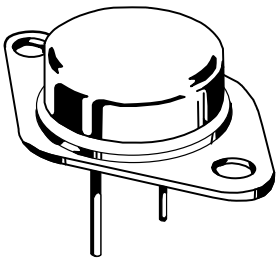


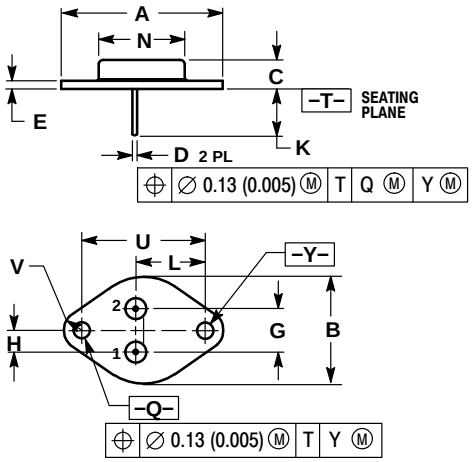

**Figure 8. “On” Voltages, MJ2955 (PNP)**



**SCALE 1:1**

**TO−204 (TO−3)**
**CASE 1−07**
**ISSUE Z**

**DATE 05/18/1988**




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO−204AA OUTLINE SHALL APPLY.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 1.550 REF | | 39.37 REF | |
| B | --- | 1.050 | --- | 26.67 |
| C | 0.250 | 0.335 | 6.35 | 8.51 |
| D | 0.038 | 0.043 | 0.97 | 1.09 |
| E | 0.055 | 0.070 | 1.40 | 1.77 |
| G | 0.430 BSC | | 10.92 BSC | |
| H | 0.215 BSC | | 5.46 BSC | |
| K | 0.440 | 0.480 | 11.18 | 12.19 |
| L | 0.665 BSC | | 16.89 BSC | |
| N | --- | 0.830 | --- | 21.08 |
| Q | 0.151 | 0.165 | 3.84 | 4.19 |
| U | 1.187 BSC | | 30.15 BSC | |
| V | 0.131 | 0.188 | 3.33 | 4.77 |

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

STYLE 2:
PIN 1. BASE
2. COLLECTOR
CASE: EMITTER

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE: DRAIN

STYLE 4:
PIN 1. GROUND
2. INPUT
CASE: OUTPUT

STYLE 5:
PIN 1. CATHODE
2. EXTERNAL TRIP/DELAY
CASE: ANODE

STYLE 6:
PIN 1. GATE
2. EMITTER
CASE: COLLECTOR

STYLE 7:
PIN 1. ANODE
2. OPEN
CASE: CATHODE

STYLE 8:
PIN 1. CATHODE #1
2. CATHODE #2
CASE: ANODE

STYLE 9:
PIN 1. ANODE #1
2. ANODE #2
CASE: CATHODE

## ADDITIONAL INFORMATION

**TECHNICAL PUBLICATIONS**:
**Technical Library:** www.onsemi.com/design/resources/technical−documentation
**onsemi Website:** www.onsemi.com

**ONLINE SUPPORT**: www.onsemi.com/support
**For additional information, please contact your local Sales Representative at** www.onsemi.com/support/sales